Additional Information for PCI 9080RDK-SH3 Users

12-23-98: Release 2.1 Rev 1 PCI SDK

This document provides additional information for users of the PCI 9080RDK-SH3 RDK.

1. Hardware and Software issues

1.1 IOP BUS

Two masters can access the local bus: the PCI 9080 and the SH7709 (SH3). When generating addresses, different modules are decoding the address lines for each of these 2 masters. The SH3 decodes its own addresses and a PLD (the Lattice chip) decodes the PCI 9080 addresses. Therefore, these two masters have a different local memory map.

The following table shows some of the memory devices present on the RDK and the respective IOP address for each master.

Memory Device	SH3 address	PCI 9080 address	Size
EPROM	0x0000 0000 + 0x2000 0000 x n (n = 0 – 6)	NA	0x0002 0000
Fujitsu FLASH MBM29LV160B	0x0100 0000 + 0x2000 0000 x n (n = 0 – 6)	NA	0x0020 0000
Fujitsu PCI BIOS FLASH MBM28F800BA	0x0200 0000 + 0x2000 0000 x n (n = 0 – 6)	0x2000 0000	0x0010 0000
PCI 9080 registers	0x0800 0000 + 0x2000 0000 x n (n = 0 – 6)	NA	0x0200
SRAM	0x0900 0000 + 0x2000 0000 x n (n = 0 – 6)	0x4000 0000	0x0004 0000
Local to PCI memory Window (through PCI 9080)	0x0A00 0000 + 0x2000 0000 x n (n = 0 – 6)	PCI 9080 decodes Direct Master memory accesses from 0x8200 0000.	0x0010 0000
Local to PCI IO Window (through PCI 9080)	0x0B00 0000 + 0x2000 0000 x n (n = 0 – 6)	PCI 9080 decodes Direct Master IO accesses from 0x8300 0000.	0x0010 0000
DRAM	0x0C00 0000 + 0x2000 0000 x n (n = 0 – 6)	NA	0x0100 0000

1.2 IOP samples

Due to the memory map issues noted above, the samples included with the PCI SDK need to be used carefully. Since all code must run on the SH3 board, all addresses specified to the linker must be SH3 addresses. For example, code running for the SRAM must be located at 0x0900 0000 (not 0x4000 0000).

IOP RAM samples, however, present a difficulty: They have to be downloadable from the PCI through the PCI 9080. Therefore, the linker directive file for these samples (RamXxx.cmd) relocates all the sections from address 0x0900 0000 to 0x4000 0000. When a PCI download occur, the host program (PLXMon 98) reads address 0x4000 0000 and downloads to it. When a serial download occurs, the IOP BSP interface converts the PCI 9080 address (from 0x4000 0000) to the SH3 address (from 0x0900 0000). This way, the code is loaded at the correct location.

IOP ROM samples use DRAM instead of SRAM except for the Scatter-Gather lists. Scatter-Gather Lists (SGL) are used for DMA. These lists have to be accessible by the PCI 9080 and therefore have to be located in the SRAM. You may notice that the SRAM address used for the ROM SGL is in conflict with the address used for the RAM samples and the Boot FLASH accesses. Therefore, it is recommended to reset the board after each time the flash is programmed or read, or after a RAM sample has returned.

Also, several embedded modules using the PCI 9080 have been added with 2 macros: TRANSLATE_CPU_TO_PLX_ADDR and TRANSLATE_PLX_TO_CPU_ADDR. These macros perform address translation and are defined in bspsh3.h. The modules affected are: the IDMA sample, the IOP API and the BSP.
***Note**: Many IOP API functions require an IOP address. All these addresses must be valid to the SH-3 CPU. The IOP API will perform translation when needed. Providing an invalid address to the SH3 will most likely fail the function.*

1.3 FLASH programming

Two flashes are present on the RDK board: A PCI BIOS flash and a Boot FLASH. The PLX RDK supports flash programming only for the Boot FLASH.

Here are a few things to keep in mind when flash programming:

- 4 switches on the back of the evaluation board select which of the EPROM or the Boot FLASH the SH3 will boot from. When shipped, the SH3 boots from the EPROM. The settings are:

Settings of DSW switches 1 2 3 4	Boot device
ON OFF OFF ON (default)	EPROM (TMS27C010A-10)
OFF ON ON OFF	Boot FLASH (MDM29LV160B)

- Only the SH3 can reprogram the flash. Therefore, in PLXMon 98, the FLASH programming method must be: IOP.
- In the PCI SDK, only the ROM samples can reprogram the flash. RAM samples cannot do it because the FLASH programming method requires the entire SRAM. RAM samples always run from the SRAM, ROM samples do not use the SRAM. Also, the Minirom sample cannot reprogram the flash.
- ROM samples have the choice of running entirely in the DRAM (code relocation) or in the boot device (no code relocation). The choice is available in the linker directive file RomXxx.cmd. FLASH programming will not be possible if the ROM sample is setup to run in the boot device and that boot device is the Boot FLASH.
- The PCI SDK does not support programming flashes with binaries larger than 256K.

2. Installation

This section presents the installation instructions necessary for building the HelloWorld sample for the PCI 9080RDK-SH3 RDK board. It assumes that you have already installed the PCI SDK software using the instructions in the PCI SDK User's Manual and that the installation directory is <PCI_SDK_INSTALL_DIR>.

1. Insert the Hitachi's HiVIEW Development Tools CD-ROM Reference Library version 1.4 CD into the CD-ROM drive.
2. Run <CD_ROM drive>:\install\setup.exe. An installation wizard should appear.
3. On the Registration window, in the Tool Chains box, select only Cygnus. Also fill out all the other required fields until you can click on Next.
4. On the Select Components Window, highlight the Tool Chains item and click on Change… A Select Sub-components dialog box should appear. Select only the Cygnus SH Tool Chain and click on Continue. Also deselect the Examples item on the first window.
5. You are now able to finish the SH tools installation.
6. Install Microsoft Visual C++ 5.0. Visual C++ 5.0 has the nmake utility necessary for building the SH3 libraries and executables.
7. Open the <PCI_SDK_INSTALL_DIR>\bin\SetSH3.bat file for editing.
8. At line 53, change the SH3_ROOT_PATH variable with the correct path. If you had installed the Hitachi tools to their default directory, the correct path should be C:\Hitachi\Tchain\Cygnus\Sh.
9. Also at line 65, add to the PATH variable the directory of the nmake utility from Microsoft Visual C++ 5.0. This directory should be <VISUAL_CPP_INSTALL_DIR>\Vc\bin.
10. Save and close the SetSH3.bat file.
11. On the Windows desktop, go to the Start menu, click on Programs, click on PLX PCISDK v2.1 Rev 1 and click on SH-3 Compiler Environment. This should open a DOS window and go to the Hello sample directory.
12. For compiling the RAM version of the Hello sample, type:
    nmake –f 80-sh3.mak
    For compiling the ROM version of the Hello sample, type:
    nmake –f 80-sh3.mak ROM="TRUE"